lecture1: Introduction to silicon photonics

Prepared by Lorenzo Pavesi
University of Trento
Photonics is the technology associated with signal generation, processing, transmission and detection where the signal is carried by photons (i.e. light).
Photonic devices produced within standard silicon factory and with standard silicon processing

i.e. CMOS compatible
Motivation to Silicon Photonics

- Limit of microelectronic evolution where photonics can help in take pace with Moore’s law
- Optical communication evolution
- A new technology platform to enable low cost and high performance photonics
the main thrust for semi business growth
“Smaller, Faster, Cheaper”
The invention of the transistor

23-12-1947

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The First Planar Transistor

1959

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The First Planar Integrated Circuit

1961

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Cramming more components onto integrated circuits

With unit cost falling as the number of component circuit rises, by 1975 economics may dictate square many as 65,000 components on a single silicon chip.

By Gordon E. Moore
Director, Research and Development Laboratories, Fairchild Semiconductors division of Fairchild Camera and Instrument Corp.

Electronics, Volume 38, Number 8, April 19, 1965
Intel 4004 Microprocessor

1971
Moore’s Law in microprocessors

2X growth in 1.96 years!

Transistors (MT)

Year


0.001  0.01  0.1  1  10  100  1000

8004  8008  8080  8086  8085  486  386  286

Pentium® proc

P6

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CMOS Scaling (ITRS Roadmap)
Die size grows by 14% to satisfy Moore’s law.
Gordon Moore Prediction Circa 1977

Moore was not always accurate

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Lead microprocessors frequency doubles every 2 years

- 8004
- 8008
- 8080
- 8085
- 8086
- 286
- 386
- 486
- P6
- Pentium ® proc

Clock Frequency

Year

Frequency (MHz)


0.1 1 10 100 1000 10000

2X every 2 years

Courtesy, Intel

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Clock Frequency

2X every 2 years

Pentium® proc

P6

Year


Frequency (MHz)

0.1 1 10 100 1000 10000

Saturation

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Today chip cross section

Figure 28  Cross-section of Hierarchical Scaling

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CPU Multi-layer Metal Increase Trend

# of Metal Layers

- 1980-2u
- 1984-1.5u
- 1987-1.0u
- 1990-0.8u
- 1993-0.6u
- 1995-0.35u
- 1997-0.25u
- 1999-0.18u
- 2001-0.13u

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...here we have a problem.....

The problem of interconnects
Interconnect length

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10 Km long interconnect

- Power dissipation
- Latency
- Delay
- ...

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Delay

RC time constants
\[ R = \rho L / A \]
\[ C = \kappa A / d \]

**Figure 2.** Calculated gate delay and wire delay as a function of the minimum feature size (device generation). From SIA Roadmap 1997 [3]. Interconnections and signal integrity, DAC tutorial. 38th Design Automation Conf. ©2001 (www.amanogawa.com/epep2000/files/jose1.pdf).
Power Dissipation

Power delivery and dissipation will be prohibitive.

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Power Density

- Rocket
- Nozzle
- Nuclear
- Reactor

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The Challenges

Power Limitations

Diminishing Voltage Scaling

Power = Capacitance x Voltage$^2$ x Frequency
also
Power $\sim$ Voltage$^3$

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The Rise of Multi-Core Architectures

- Rise of parallel multi-core architectures to mitigate power dissipation
- Parallel architectures with multiple simpler processing cores provide better performance per watt than architectures based on a single complex processor
- State-of-the-art commercial chips feature more parallel and distributed architectures that are essentially multi-core chips
  - Montecito (Intel)
  - Cell (IBM, Toshiba, Sony)
- Key is to design robust, scalable, fast, and power-efficient: intra-chip communication networks

(58)
Tera-leap to Parallelism:

Era of Tera-Scale Computing

More performance Using less energy

The days of single-core chips

All this compute capability may require high speed optical links

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Chip Multiprocessors

### IBM Cell:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology process</td>
<td>90nm SOI with low-κ dielectrics and 8 metal layers of copper interconnect</td>
</tr>
<tr>
<td>Chip area</td>
<td>235mm²</td>
</tr>
<tr>
<td>Number of transistors</td>
<td>~234M</td>
</tr>
<tr>
<td>Operating clock frequency</td>
<td>4GHz</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>~100W</td>
</tr>
<tr>
<td>Percentage of power dissipation due to global interconnect</td>
<td>30-50%</td>
</tr>
<tr>
<td>Intra-chip, inter-core communication bandwidth</td>
<td>1.024 Tbps, 2Gb/sec/lane (four shared buses, 128 bits data + 64 bits address each)</td>
</tr>
<tr>
<td>I/O communication bandwidth</td>
<td>0.819 Tbps (includes external memory)</td>
</tr>
</tbody>
</table>

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Interconnects pose problems not only within the chip.

Growth of the Internet

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Power due to the explosion of internet

Power Consumption Problem

- Single Shelf
  - Throughput: 1.2 Tbps
  - Power: ~15kW

- Multiple Shelves
  - Throughput: 92 Tbps
  - Power: >1 MegaW

- 80 Shelves
  - Additional 1 MegaW for cooling central office

Google’s new data centers
- Power consumption > 100 MegaW

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To solve the interconnect problem

GO TO PHOTONICS

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Scaling Optoelectronic-VLSI Circuits into the 21st Century: A Technology Roadmap

Ashok V. Krishnamoorthy, Member, IEEE, and David A. B. Miller, Fellow, IEEE

Reasons for Optical interconnects

Scaling problem of electrical interconnects

• optics completely avoids this problem (no comparable resistive loss physics)

Other quantitative reasons for optics

• increased density for long distance interconnections (e.g., off-chip and off-board)
• precision of synchronization
• might give faster interconnects on chip
• possible power savings

Qualitative reasons for optics

• voltage isolation, absence of frequency-dependent crosstalk
• design simplification
  – e.g., avoid transmission line design problems, inductance

4/2/2003

David A. B. Miller, Stanford
Length Scales for interconnects

- **FR4**: Chip to Chip (1–50 cm) and Board to Board (50–100 cm)
- **Copper/Fiber**: Rack to Rack (1 to 100 m)
- **Fiber**: Sonet (0.1–80 km) and Fiber Channel

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Moving to Interconnects

Chip to Chip
1 – 50 cm

Board to Board
50 – 100 cm

Rack to Rack
0.1 – 80 km

Metro & Long Haul

Decreasing Distances

Optical

Copper

Billions

Millions

Thousands

Volumes

Drive optical to high volumes and low costs

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Optical interconnects

Today
Optical connection between individual computers are commercially available.

2-5 Years
Optical communications will enter the computer, connecting one circuit board to another.

5-10 Years
Chip-to-chip communications will enter the market.

15+ Years
Experts disagree on whether optical interconnects will ever connect the subsystems within a chip.

Source: IEEE spectrum

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Evolution of optical communication
Brief story of optical communication

1958-59 Kapany creates optical fiber with cladding
1960-Ted Maiman demonstrates first laser in Ruby
1962-4 Groups simultaneously make first semiconductor lasers
1970-First room temp. CW semiconductor laser-Hayashi & Panish
April 1977-First fiber link with live telephone traffic-GTE Long Beach 6 Mb/s
May 1977-First Bell system 45 mb/s links 850nm MM
Early 1980s-InGaAsP 1.3 µm Lasers
- 0.5 dB/km, lower dispersion-Single mode
Late 1980s-Single mode transmission at 1.55 µm - 0.2 dB/km
1989-Erbium doped fiber amplifier
1 Q 1996- 8 Channel WDM

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Source: Tingye Li, AT&T Research Laboratories; Alan E. Willner
Evolution of optical data link

- Optical fiber system has the capacity to hold the whole internet traffic.
- It doubles each 9 months vs Moore’s law 18 months.

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In 2000, for the first time, semiconductor revenues in communication exceeded revenues in PC sector.

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The next challenge

Bandwidth bottleneck in metro optical networks

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### Major limit of photonics

#### Technology Comparison: Optics vs. ICs

<table>
<thead>
<tr>
<th>Technologies</th>
<th>Optical Components</th>
<th>Semiconductor IC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Repeatable building block</td>
<td>None (LD, PD, Mod, Filter, Isolator...)</td>
<td>Transistors</td>
</tr>
<tr>
<td>Uniform material base</td>
<td>None (InP, GaAs, Si...)</td>
<td>Silicon</td>
</tr>
<tr>
<td>Dominant manufacturing process</td>
<td>None (Hybrid, monolithic, active, passive...)</td>
<td>CMOS</td>
</tr>
</tbody>
</table>

Source: J. P. Morgan

No standardized technology for optical components manufacturing

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Figure 1. Tunable optical transmitter integrated in a polymer optical bench platform.
Innovation driven by cost

![Diagram showing cost vs. functionality with Discretes, Hybrids, and Monolithic categories.](image)

The inevitable technology evolution needed to satisfy market

Functionality (range, accuracy, speed, size)

Figure 1

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<table>
<thead>
<tr>
<th>Material</th>
<th>$\lambda$ (μm)</th>
<th>Band gap</th>
<th>$\Delta n/n$ (%)</th>
<th>Tx</th>
<th>Rx</th>
<th>waveguides</th>
<th>Optical component</th>
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<tbody>
<tr>
<td>Si</td>
<td>1.1</td>
<td>I</td>
<td>70</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>GaAs</td>
<td>0.8</td>
<td>D</td>
<td>0-14</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>InP/InGaAs</td>
<td>1.55</td>
<td>D</td>
<td>0-3</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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</tbody>
</table>
Big challenges

- How to merge photonics and electronics
- How to move optical communication to the chip
- How to standardize photonics
- How to
Big challenges

- How to merge photonics and electronics
- How to move optical communication to the chip
- How to standardize photonics
- How to

Silicon photonics solution to these challenges?

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Why do we want to use silicon

Because silicon is an optical material
### General properties at room T

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atomic weight</td>
<td>28.09</td>
<td></td>
</tr>
<tr>
<td>Atomic density</td>
<td>4.99x10^14</td>
<td>atoms/cm^3</td>
</tr>
<tr>
<td>Boiling point</td>
<td>2,078</td>
<td>°C</td>
</tr>
<tr>
<td>Breakdown field</td>
<td>-3x10^5</td>
<td>V/cm</td>
</tr>
<tr>
<td>Bulk modulus</td>
<td>7.7x10^11</td>
<td>dynes/cm^2</td>
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<tr>
<td>Burgers vector</td>
<td>0.374</td>
<td></td>
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<tr>
<td>Compliance &lt;111&gt;^b</td>
<td>5.32x10^13</td>
<td>cm^2/dyne</td>
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<tr>
<td>Covalent radius</td>
<td>0.118</td>
<td>nm</td>
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<tr>
<td>Critical density [1]</td>
<td>0.1207</td>
<td>g/cm^3</td>
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<td>Critical pressure [1]</td>
<td>530</td>
<td>atm</td>
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<tr>
<td>Critical temperature [1]</td>
<td>4,888</td>
<td>°C</td>
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<tr>
<td>Critical volume [1]</td>
<td>232.6</td>
<td>cm^3/g/mol</td>
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<td>Crystal plane spacing (100)</td>
<td>0.543</td>
<td>nm</td>
</tr>
<tr>
<td>(110)</td>
<td>0.383</td>
<td>nm</td>
</tr>
<tr>
<td>(111)</td>
<td>0.313</td>
<td>nm</td>
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<tr>
<td>Crystal structure</td>
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<td>Density</td>
<td>2.33</td>
<td>g/cm^3</td>
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<tr>
<td>Density of surface atoms (100)</td>
<td>6.78x10^14</td>
<td>atoms/cm^3</td>
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<tr>
<td>(110)</td>
<td>9.59x10^14</td>
<td>atoms/cm^3</td>
</tr>
<tr>
<td>(111)</td>
<td>7.82x10^14</td>
<td>atoms/cm^3</td>
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<tr>
<td>Dielectric constant</td>
<td>11.8</td>
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<tr>
<td>Effective density of states</td>
<td></td>
<td></td>
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<tr>
<td>Conduction band</td>
<td>3.22x10^19</td>
<td>n/cm^3</td>
</tr>
<tr>
<td>Valence band</td>
<td>1.82x10^19</td>
<td>n/cm^3</td>
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<tr>
<td>Elastic constant</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{11}</td>
<td>1.99x10^12</td>
<td></td>
</tr>
<tr>
<td>C_{12}</td>
<td>0.483x10^12</td>
<td></td>
</tr>
<tr>
<td>C_{14}</td>
<td>0.671x10^12</td>
<td></td>
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<tr>
<td>Electron affinity (111)^b</td>
<td>4.85</td>
<td>eV</td>
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<table>
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<tr>
<th>Property</th>
<th>Value</th>
<th>Units</th>
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<tbody>
<tr>
<td>Electron effective mass at 49K^a</td>
<td>0.98</td>
<td></td>
</tr>
<tr>
<td>Longitudinal (m/m_0)</td>
<td>0.19</td>
<td></td>
</tr>
<tr>
<td>Transverse (m/m_0)</td>
<td>1.08</td>
<td></td>
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<tr>
<td>Energy gap (see fig. 1.6)</td>
<td>1.12</td>
<td>eV</td>
</tr>
<tr>
<td>Hardness</td>
<td>7</td>
<td>Moh</td>
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<tr>
<td>Heat capacity [1]</td>
<td>4.76</td>
<td>cal/gmol°C</td>
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<td>Heat of fusion @ m.p. [1]</td>
<td>264</td>
<td>cal/g</td>
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<td>Heat of sublimination @ m.p. [1]</td>
<td>4,075.0</td>
<td>cal/g</td>
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<tr>
<td>Heat of vaporization @ m.p. [1]</td>
<td>3,812.0</td>
<td>cal/g</td>
</tr>
<tr>
<td>Hole effective mass at 4K^f</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Heavy (m/m_0)</td>
<td>0.537</td>
<td></td>
</tr>
<tr>
<td>Light (m/m_0)</td>
<td>0.153</td>
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<tr>
<td>Density of states (m/m_0)</td>
<td>0.591</td>
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<tr>
<td>Intrinsic carrier concentration (see fig. 1.7)</td>
<td>n_p</td>
<td>1.38x10^19</td>
</tr>
<tr>
<td></td>
<td>n_n</td>
<td>1.90x10^20</td>
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<tr>
<td>Intrinsic Debye length L_D</td>
<td>28.7</td>
<td>nm</td>
</tr>
<tr>
<td></td>
<td>4.0x10^4</td>
<td>nm</td>
</tr>
<tr>
<td>Intrinsic resistivity</td>
<td>2.3x10^5</td>
<td>Ω-cm</td>
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<tr>
<td>Lattice constant</td>
<td>0.545</td>
<td>nm</td>
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<td>Liquid density @ m.p. [1]</td>
<td>2.33</td>
<td>g/cm^3</td>
</tr>
<tr>
<td>Liquid heat capacity @ m.p. [1]</td>
<td>6.755</td>
<td>cal/gmol°C</td>
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<tr>
<td>Liquid thermal capacity @ m.p. [1]</td>
<td>1.025x10^5</td>
<td>cal/sec-cm-°C</td>
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<tr>
<td>Liquid viscosity @ m.p. [1]</td>
<td>0.88</td>
<td>zeptipoise</td>
</tr>
<tr>
<td>Melting point [1]</td>
<td>1,412.2</td>
<td>°C</td>
</tr>
<tr>
<td>Minority carrier lifetime</td>
<td>2.5x10^4</td>
<td>s</td>
</tr>
<tr>
<td>Nearest neighbor distance</td>
<td>0.235</td>
<td>nm</td>
</tr>
<tr>
<td>Percent expansion on freezing @ m.p. [1]</td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>Poisson's ratio</td>
<td>0.57</td>
<td></td>
</tr>
<tr>
<td>Refractive index</td>
<td>3.4</td>
<td></td>
</tr>
<tr>
<td>Scattering limited velocity Electron Hole</td>
<td>~1.0x10^7</td>
<td>cm/s</td>
</tr>
<tr>
<td></td>
<td>~8.4x10^8</td>
<td>cm/s</td>
</tr>
<tr>
<td>Shear modulus</td>
<td>7.55x10^11</td>
<td>dynes/cm^2</td>
</tr>
<tr>
<td>Surface tension @ m.p. [1]</td>
<td>736</td>
<td>dynes/cm</td>
</tr>
<tr>
<td>Symbol</td>
<td>Si</td>
<td></td>
</tr>
<tr>
<td>Thermal conductivity [1]</td>
<td>0.353</td>
<td>cal/sec-cm-°C</td>
</tr>
<tr>
<td>Torsion modulus</td>
<td>5.97x10^11</td>
<td>dynes/cm^2</td>
</tr>
</tbody>
</table>
Silicon is an Excellent Optical Material

High refractive index difference with SiO₂

- $n_{Si} = 3.5$
- $n_{SiO₂} = 1.45$

Source: UCLA

*Source: Silicon Photonics – PhD course prepared within FP7-224312 Helios project*
Silicon is easily shaped

- ultra-compact waveguides
- features: 50-500 nm ± 1-10 nm
- fabrication in CMOS fab (deep UV lithography)
IC’s are made of Silicon (>98%) even for high frequency applications (cellular phone)
Silicon is cheaper than other semiconductors

<table>
<thead>
<tr>
<th></th>
<th>Wafer size (R&amp;D)</th>
<th>Wafer size (commercial)</th>
<th>Wafer cost (€)</th>
<th>mm² substrate cost (€)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>450 mm</td>
<td>300 mm</td>
<td>100</td>
<td>0.001</td>
</tr>
<tr>
<td>SOI</td>
<td>?</td>
<td>300 mm</td>
<td>800</td>
<td>0.008</td>
</tr>
<tr>
<td>InP</td>
<td>150 mm</td>
<td>100 mm</td>
<td>300</td>
<td>0.03</td>
</tr>
<tr>
<td>GaAs</td>
<td>200 mm</td>
<td>150 mm</td>
<td>300</td>
<td>0.013</td>
</tr>
</tbody>
</table>
Mature and widespread technology
Silicon limit

Indirect band gap =
low radiative recombination probability = long radiative lifetimes (ms)

- Free carriers move around =
Non-radiative recombinations prevail
- Extremely low internal quantum efficiency in bulk silicon (10^-6)
Silicon Pro’s and Cons

- Transparent in 1.3-1.6 μm region
- CMOS compatibility
- Low cost
- High-index contrast – small footprint

- No electro-optic effect
- No detection in 1.3-1.6 μm region
- High index contrast – coupling
- Lacks efficient light emission

Silicon will not win with passive devices.
Must produce active devices that add functionality
Success of electronics?

Integrated circuits

- economics of wafer scale integration
- performance (smaller is faster!)
- miniaturization in its own right
- complex function can be made by a limited number of high-yield processes
  - focus on one production technology
  - few companies in the food chain
- all efforts on the same material = Silicon

Can we repeat this success with Silicon Photonics?

All those who have posted beautiful images and slides on the internet which I have re-used here